

Comprehensive Experimental Investigation of Gate Current Limitation Effects on Power GaAs FETs RF Performances

N. Constantin and F.M. Ghannouchi. "Comprehensive Experimental Investigation of Gate Current Limitation Effects on Power GaAs FETs RF Performances." 1995 MTT-S International Microwave Symposium Digest 95.2 (1995 Vol. II [MWSYM]): 717-720.

This paper presents for the first time a detailed experimental investigation of gate current limitation effects on power GaAs FETs RF performances. This gate current limitation is entirely accomplished by dynamic compensation of the gate bias voltage. Effects of this current limitation on power added efficiency and output power performance have been examined through an extensive experimental investigation over the entire Smith chart. Comprehensive results are given and allow to determine the optimal resistor value needed for the gate current limitation. Thermal runaway problem is also taken into consideration when selecting the gate resistor.

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